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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,138	03/06/2001	Hyae-Ryoung Lee	5649-553DV	7287

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,138	LEE, HYAE-RYOUNG	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35,36 and 38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35,36 and 38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/103,970* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 42 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. With regard to claim 42, the recitation of "the dielectric layer" in line six of the claim is not clear. To what dielectric layer is this recitation referring? For purposes of this office action "the dielectric layer" will be considered -- the second dielectric layer--.

4. It is not clear in claim 42 if "a multilayer bonding pad" in the last line of the claim is the same as "a bonding pad" of claim 35. Are there two bonding pads in the claim? How might these two bonding pads be related?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 35, 36, and 38 – 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato (USPAT 5739587).

With regard to claim 35, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 a method of forming a bonding pad for an integrated circuit. Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 forming a dielectric layer (60) having first and second opposing faces on an integrated circuit substrate (10), the dielectric layer including a closed via (102/45) therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer. Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 forming a conductive pattern in the closed via and on the dielectric layer opposite the substrate.

With regard to claim 36, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 wherein the step of forming the conductive pattern comprises the step of forming the conductive pattern filling the closed via and on the dielectric layer opposite the substrate.

With regard to claim 38, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 wherein the closed via is of a circular via.

With regard to claim 39, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 wherein the step of forming a dielectric layer comprises the step of forming the dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via and an open via therein. Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 wherein the step of forming the conductive pattern comprises the step of forming the conductive pattern in the closed via, in the open via and on the dielectric layer opposite the substrate.

With regard to claim 40, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 a method of forming a bonding pad for an integrated circuit. Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 forming a dielectric layer (60) having first and second opposing faces on an integrated circuit substrate (10), the dielectric layer including a closed via (102) therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer, wherein the closed via penetrates through the dielectric layer and extends towards the integrated circuit substrate. Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40

forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

With regard to claim 41, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 wherein the step of forming the conductive pattern comprises forming the conductive pattern in the closed via and on the dielectric layer opposite the substrate, wherein the conductive pattern penetrates through the dielectric layer and extends towards the integrated circuit substrate.

With regard to claim 42, Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 wherein the dielectric layer comprises a first dielectric layer (540) and the conductive pattern comprises a first conductive pattern (530) and the closed via comprises a first closed via (102/611). Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 forming a second dielectric layer (520) having first and second opposing faces on the first conductive pattern, the second dielectric layer including a second closed via (102/601) therein that extends from the first face of the second dielectric layer to the second face of the second dielectric layer and that encloses an inner portion of the second dielectric layer, and is enclosed by an outer portion of the second dielectric layer. Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 forming a second conductive pattern on the second dielectric layer that extends from the first face of the second dielectric layer to the second face of the second dielectric layer in the second closed via and on the second dielectric layer opposite the substrate to form a multilayer bonding pad (510) on the integrated circuit substrate.

Response to Arguments

7. Applicant's arguments filed January 13, 2003 have been fully considered but they are not persuasive.

8. With regard to the applicant's argument that "Figures 1 – 3 of Sato do not disclose all of the recitations of independent claim 35 as required under section 102," nowhere in the rejections has it been suggested that all of the recitations of independent claim 35 are shown exclusively figures 1 – 3 of Sato. In fact the rejections cite "Sato discloses in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40," and while a reference must be considered as a whole, no argument against only figures 1 – 3 of Sato can be considered complete or persuasive. Therefore, the applicant's arguments are not persuasive and the rejection is proper.

9. With regard to the applicant's argument that "conductors 102 and 103 shown in Figure 8 [of Sato] are grooves in the upper electrode layer 100," nowhere in Sato is a conductive material formed within grooves in an upper electrode layer. Attention should be drawn to column 3, lines 31 – 44 stating that all of figures 4 – 9c show embodiments of a conductor layout. Further, in Sato lines 5 and 6 of column 6 states "The layout of interlayer connection conductors (e.g., planar pattern) will be described below." The "interlayer connection conductors" are shown in figures 3 and 4 as elements 40 – 45 disposed in interlayer insulation film 60. The "described below" in column 6, lines 7 – 44 describe figures 4 – 9c. The citation made by the applicant,

with regard to figure 8, is included in this "described below" section. After a careful and thorough review of this section there is no doubt that Sato is describing different embodiments of conductor patterns in a dielectric layer (an interlayer insulation film in Sato). It is clear from the disclosure of Sato in figures 3, 8 and 11, the abstract, lines 3 – 8 and 13 – 15, column 3, lines 31 – 40 and column 6, lines 7 – 12 and 36 – 40 that conductors 102, 103, and 104 are formed in a dielectric layer. Therefore, the arguments are not persuasive and the rejection is proper.

10. With regard to the applicant's arguments that "even assuming for the sake of argument that the conductors 102 and 103 shown in Figure 8 did pass through the upper electrode layer 100, such a structure still would still not disclose all the recitations of independent Claims 35 and 40," is not understood because conductors passing through the upper electrode layer is not claimed or suggested in the rejection or in Sato. The claims are drawn towards conductors passing through an interlayer insulating film, or a dielectric, and that is what Sato is relied upon in the rejection as teaching. Sato discloses all of the claim limitations. Therefore, the arguments are not persuasive and the rejection is proper.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
February 24, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800